UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/972,319	10/05/2001	Warren Snyder	CYPR-CD00179	4114

7590 09/16/2004

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, CA 95113

EXAMINER	
MASKULINSKI, MICHAEL C	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 09/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/972,319	SNYDER, WARREN	
	Examiner	Art Unit	
	Michael C Maskulinski	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-15* is/are allowed.

6)☒ Claim(s) *1,2,7 and 16-19* is/are rejected.

7)☒ Claim(s) *3-6, 20 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/21/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Non-Final Office Action

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. Claims 18 and 19, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claims 18 and 19 recite the limitation "said second memory". There is insufficient antecedent basis for this limitation in the claim. For purposes of examination the Examiner has interpreted claim 19 as being dependent on claim 17, which discloses a second memory.

4. Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps of a method and structural cooperative relationships of elements, such omission amounting to a gap between the necessary steps and structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships and steps are: "said test instructions" are stored in a first memory not in a second memory as claimed (see claim 16). It is unclear as to how the second memory now contains test instructions that were stored in a first memory. Further, if claim 18 were dependent on claim 17, as interpreted above, then "said test instructions" would be "program instructions."

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 2, 7, 16, and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Satoh, US 2001/0010083 A1.

Referring to claim 1:

a. In paragraph 0026, Satoh discloses that when the external circuit inspection device is connected to the inspection information interface to switch the operation mode of the bus control unit from the normal mode to the inspection mode, the bus control circuit switches a destination to be connected to the central processing unit from the external bus to the inspection control circuit at a given time (entering a test mode establishing said microprocessor as a slave and a test controller as a master).

b. In Figure 3 and in paragraph 0027, Satoh discloses that the central processing unit reads the instruction codes and data to be processed from the inspection control circuit at a predetermined time. Therefore, if desired instruction codes and data to be processed are stored into the registers of the inspection control circuit by the circuit inspection device, the central processing unit can

perform a desired data processing operation in the inspection mode (bypassing a first memory coupled to said microprocessor and forcing said microprocessor to execute instructions from an instruction queue).

c. In paragraph 0055, Satoh discloses that the debugging I/F of JTAG is connected to the TAP controller, the instruction register, the register unit, and the IR decoder, and carries input data "TRST", "TCK", "TMS", "TDI", etc. and output data "TDO", etc. (said test controller filling said instruction queue with instructions to be executed, said instructions originating from a test interface).

Referring to claim 2, in paragraph 0050, Satoh discloses the test interface to be JTAG (said test interface is serial).

Referring to claim 7, in paragraph 0026, Satoh discloses that in the normal mode, the bus control unit connects the external bus continuously to the central processing unit. The central processing unit reads the instruction codes and data to be processed from an external information storage medium, and executes various data processing tasks (said first memory is for holding instructions to be executed by said microprocessor when not in said test mode).

Referring to claim 16:

a. In paragraph 0026, Satoh discloses that when the external circuit inspection device is connected to the inspection information interface to switch the operation mode of the bus control unit from the normal mode to the inspection mode, the bus control circuit switches a destination to be connected to the central processing unit from the external bus to the inspection control circuit

at a given time (entering a test mode establishing said microprocessor as a slave and a test controller as a master).

b. In paragraph 0057, Satoh discloses debug control data stored by the debug control register (said test controller transferring to a queue an instruction to be executed in said microprocessor).

c. In paragraphs 0059-0061 Satoh teaches said instruction causing at least one test instruction from a first memory to be executed by said microprocessor. Further, in paragraph 0053, Satoh discloses a plurality of monitor registers for storing instruction codes for the CPU core (said first memory comprising a plurality of test instructions).

Referring to claim 17, in paragraph 0026, Satoh discloses that in the normal mode, the bus control unit connects the external bus continuously to the central processing unit. The central processing unit reads the instruction codes and data to be processed from an external information storage medium, and executes various data processing tasks. Further, in paragraph 0026, Satoh discloses switching from normal mode to test inspection mode (bypassing a second memory coupled to said microprocessor and forcing said microprocessor to execute instructions from said queue, said second memory comprising program instructions to be run when not in said test mode).

Allowable Subject Matter

7. Claims 3-6, 20, and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 8-15 are allowed.

9. The following is a statement of reasons for the indication of allowable subject matter: the prior art does not teach or reasonably suggest an instruction queue coupled to a microprocessor with instructions loaded by a test controller received from a test interface and a first memory coupled to said microprocessor, said first memory comprising pre-determined test instructions.

10. Claims 19-20 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 2004/0153802 A1	Kudo et al.
US 2002/0059543 A1	Cheng et al.
U.S. Patent 6,754,849	Tamura
U.S. Patent 6,728,902 B2	Kaiser et al.
U.S. Patent 6,728,900 B1	Meli
U.S. Patent 5,544,311	Harenberg et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (703) 308-6674. After October 15, 2004, the examiner can be reached at telephone number: (571) 272-3649. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MM

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100